Amendments to the Claims:

1. (Currently Amended) A computer implemented method of modeling the static timing behavior a combinatorial gate comprising:

~~providing~~ determining that a data signal has been propagated to a first input of [[at]] the combinatorial gate;

~~providing~~ determining that a clock signal has been propagated to a second input of [[at]] the combinatorial gate; [[and,]]

propagating the clock signal as an output signal of the combinatorial gate when the output of the combinatorial gate feeds into a clock input of a sequential circuit ~~corresponds to the clock signal~~; [[and,]]

propagating the data signal as an output signal of the combinatorial gate when the output of the combinatorial gate feeds into a data input of a dynamic circuit ~~corresponds to the data signal, the propagating the data signal modeling a near domino function~~; and

providing a static timing model of the combinatorial gate.

2. (Currently Amended) The method of claim 1 ~~wherein~~ further comprising:

~~the near domino function is propagated based upon~~ performing a reverse traversal function on a circuit design containing the combinatorial gate.

3. (Currently Amended) The method of claim 1 wherein:

~~the near domino function~~ propagating the data signal includes causing a later arriving edge of the data signal to cause the output signal to respond.

4. (Currently Amended) The method of claim 1 wherein:

the data signal includes a single edge per clock period; and,

when propagating the data signal ~~providing the near domino function~~, the single edge is propagated through the combinatorial gate.

5. (Original) The method of claim 1 wherein:

the clock signal includes two edges per clock period; and,

when propagating the clock signal, the two edges are propagated through the combinatorial gate.

6. (Currently Amended) A method of classifying ~~determining how to model~~ a combinatorial gate where the combinatorial gate receives a data signal and a clock signal comprising:

performing a reverse traversal function on a circuit containing the combinatorial gate[[,]];

~~modeling an output of the combinatorial gate as the clock signal when an input to a next element of the circuit is a clock; and,~~

~~modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data signal.~~

classifying the combinatorial gate as a clock gate when the output of the combinatorial gate is tied to a clock input of a sequential circuit; and

classifying the combinatorial gate as a near domino gate when the output of the combinatorial gate is tied to a data input of a dynamic circuit.

7. (Canceled)

8. (Currently Amended) The method of claim 7 wherein:

~~the near domino function includes~~ classifying the combinatorial gate as a near domino gate further comprises causing a later arriving edge of the data signal to cause the output signal to respond.

9. (Currently Amended) The method of claim 7 wherein:

the data signal includes a single edge per clock period; and,

when classifying the combinatorial gate as a near domino gate ~~providing the near domino function~~, the single edge is propagated through the combinatorial gate.

10. (Currently Amended) The method of claim 7 wherein:

the clock signal includes two edges per clock period; and,

when classifying the combinatorial gate as a clock gate ~~propagating the clock signal~~, the two edges are propagated through the combinatorial gate.

11-15. (Canceled)

16. (Original) A static timing engine comprising:

a data model, the data model including a combinational block determinator module, the combinational block determinator module including means for performing a reverse traversal function on a circuit containing the combinatorial gate, and a timing engine portion coupled to the data model, the timing engine portion including means for modeling an output of the combinatorial gate as a clock signal when an input to a next element of the circuit is clock input; and,

means for modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data input.

17. (Currently Amended) The static timing engine of claim 16 wherein:

the means for modeling the output of the combinatorial gate as a data signal includes means for modeling a near domino gate ~~function~~.

18. (Currently Amended) The static timing engine of claim 17 wherein:

the near domino gate ~~function~~ includes causing a later arriving edge of the data signal to cause the output signal to respond.

19. (Currently Amended) The static timing engine of claim 17 wherein:

the data signal includes a single edge per clock period; and,

when providing the near domino gate ~~function~~, the single edge is propagated through the combinatorial gate.

20. (Original) The static timing engine of claim 17 wherein:

the clock signal includes two edges per clock period; and,

when propagating the clock signal, the two edges are propagated through the combinatorial gate.